FIG. 1

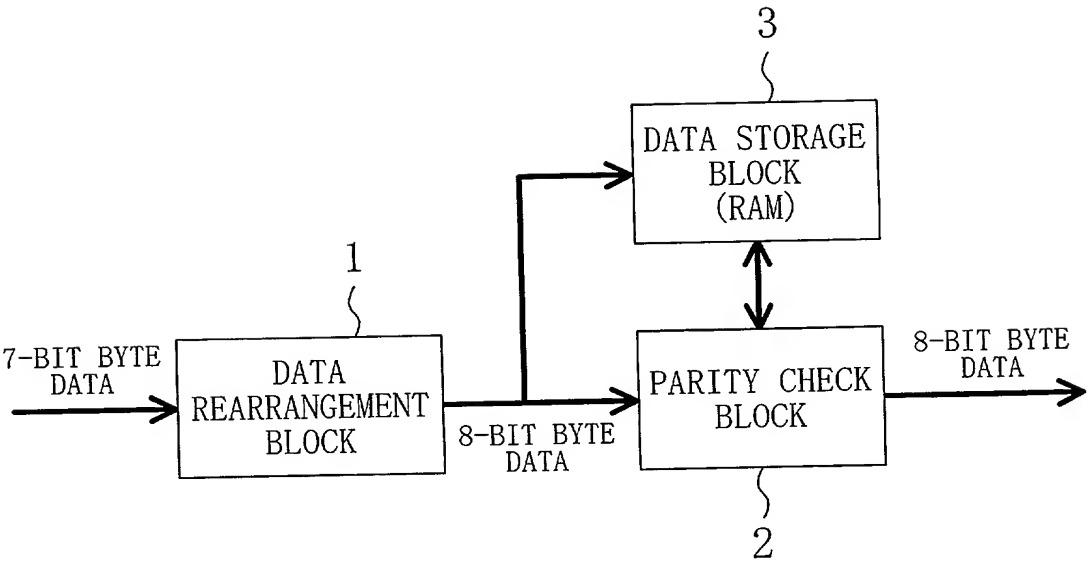
3
DATA STORAGE BLOCK (RAM)
1
7-BIT BYTE DATA
DATA REARRANGEMENT BLOCK
8-BIT BYTE DATA
PARITY CHECK BLOCK
8-BIT BYTE DATA
2

FIG. 2

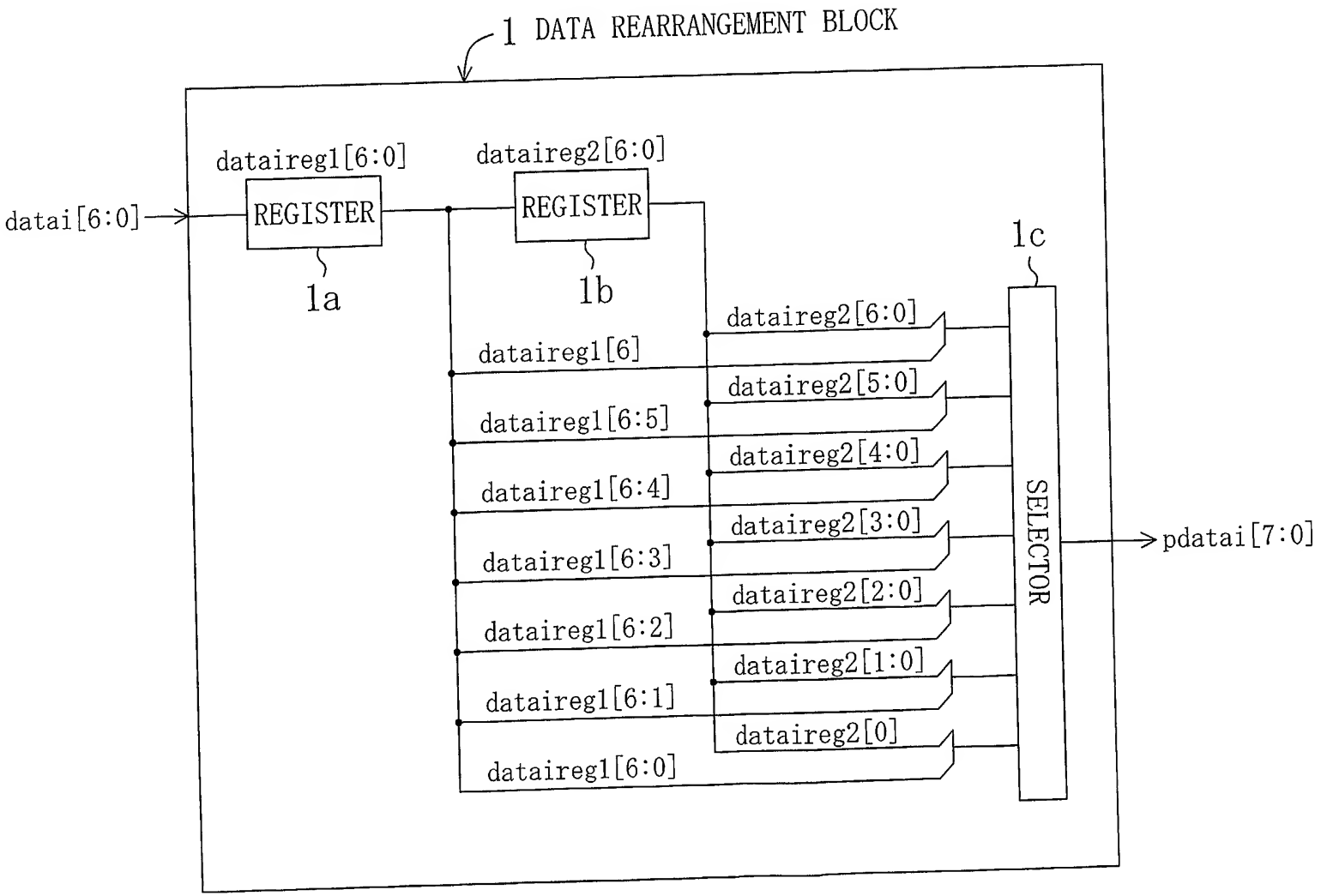
1 DATA REARRANGEMENT BLOCK
datai[6:0]
dataireg1[6:0]
REGISTER
1a
dataireg2[6:0]
REGISTER
1b
1c
dataireg2[6:0]
dataireg1[6]
dataireg2[5:0]
dataireg1[6:5]
dataireg2[4:0]
dataireg1[6:4]
dataireg2[3:0]
dataireg1[6:3]
dataireg2[2:0]
dataireg1[6:2]
dataireg2[1:0]
dataireg1[6:1]
dataireg2[0]
dataireg1[6:0]
SELECTOR
pdatai[7:0]

FIG. 3

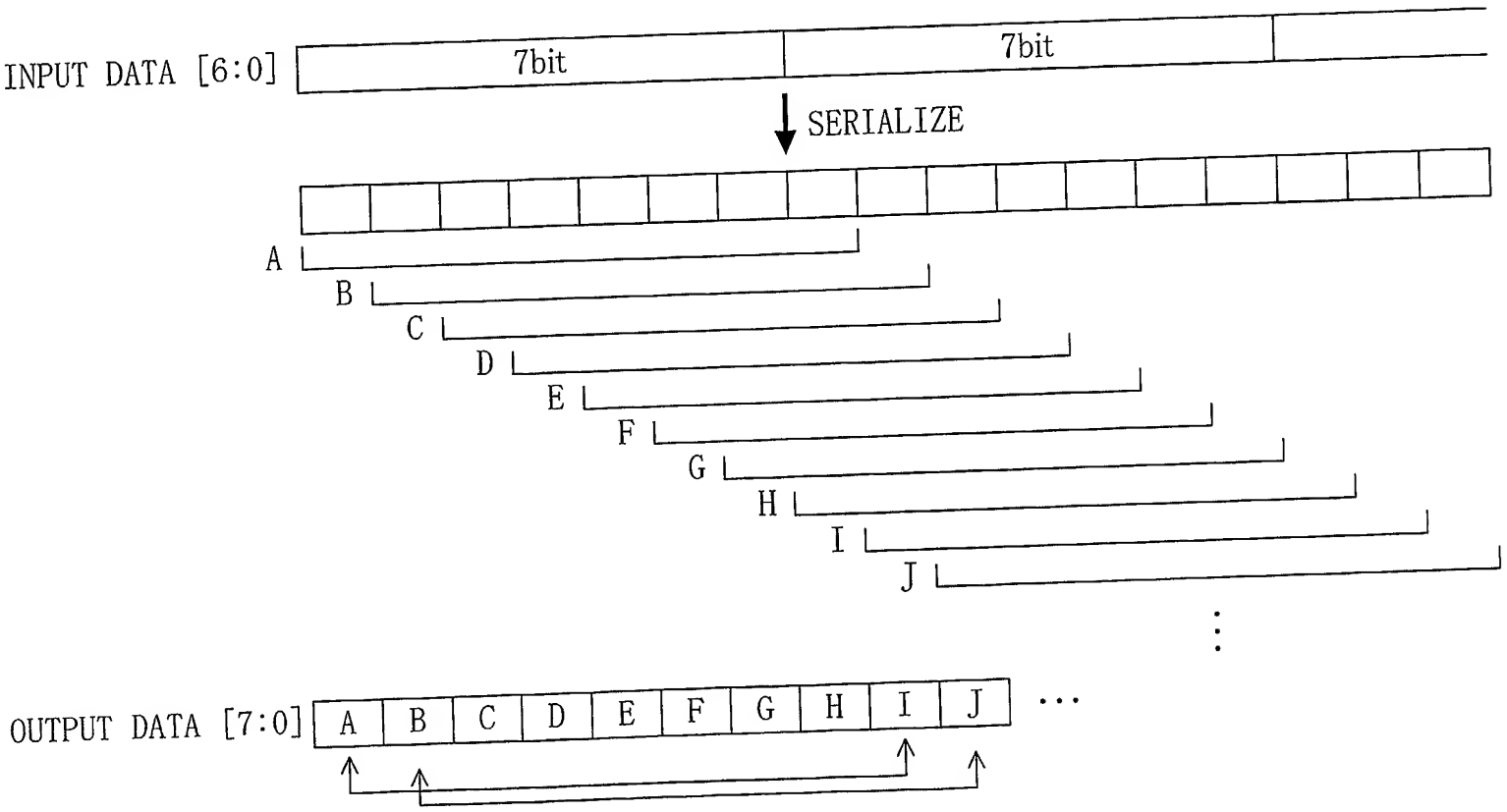
INPUT DATA [6:0]
7bit
7bit
SERIALIZE
A
B
C
D
E
F
G
H
I
J
OUTPUT DATA [7:0]
A
B
C
D
E
F
G
H
I
J

FIG. 4

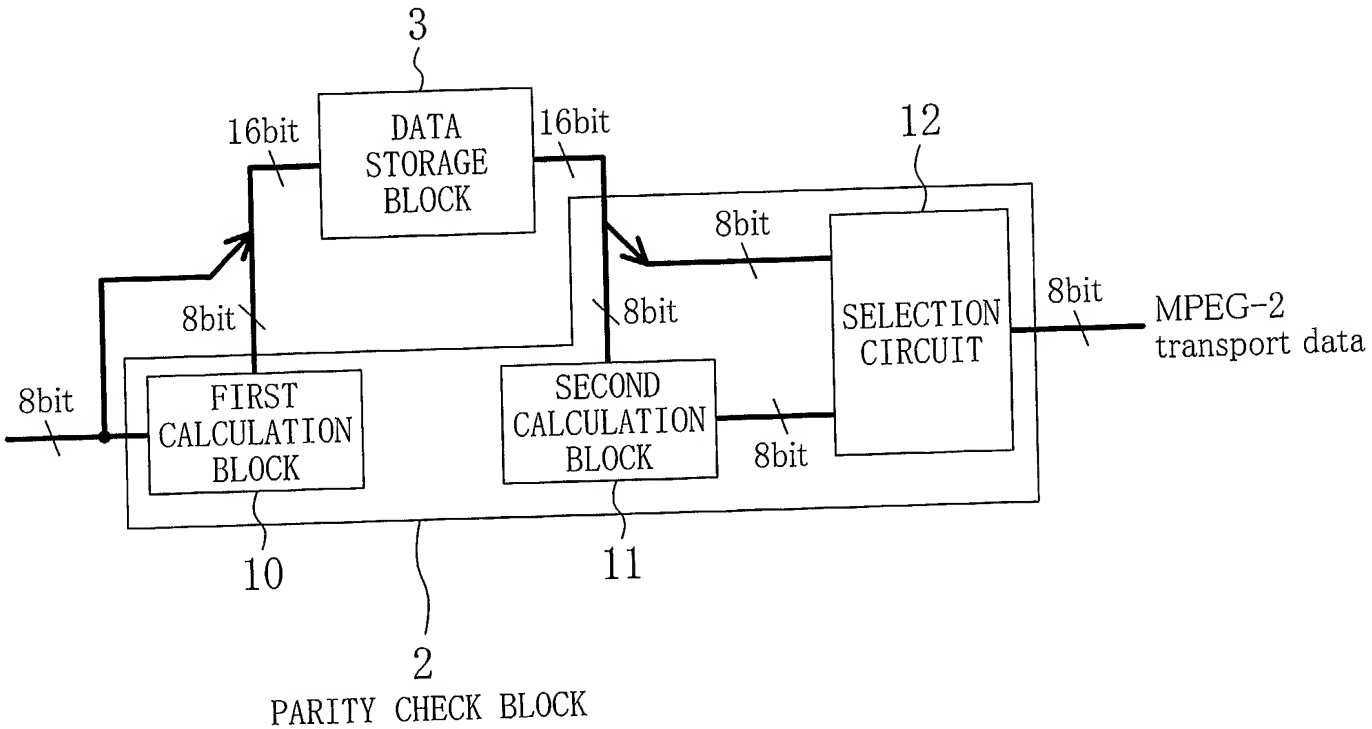
3
16bit
DATA STORAGE BLOCK
16bit
12
8bit
8bit
8bit
SELECTION CIRCUIT
8bit
MPEG-2 transport data
8bit
FIRST CALCULATION BLOCK
SECOND CALCULATION BLOCK
8bit
10
11
2
PARITY CHECK BLOCK

FIG. 5

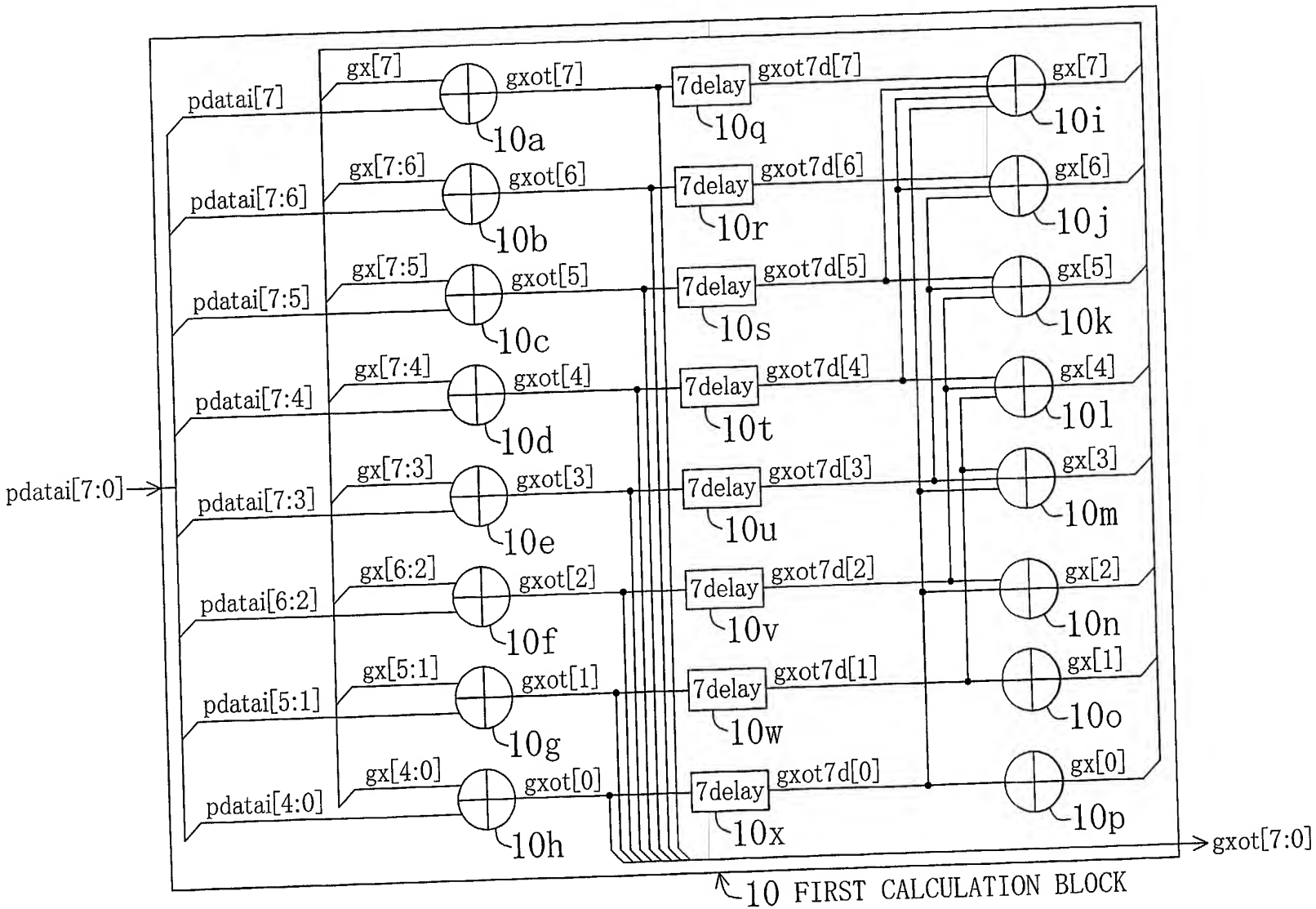
pdatai[7:0]
pdatai[7]
pdatai[7:6]
pdatai[7:5]
pdatai[7:4]
pdatai[7:3]
pdatai[6:2]
pdatai[5:1]
pdatai[4:0]
gx[7]
gx[7:6]
gx[7:5]
gx[7:4]
gx[7:3]
gx[6:2]
gx[5:1]
gx[4:0]
gxot[7]
gxot[6]
gxot[5]
gxot[4]
gxot[3]
gxot[2]
gxot[1]
gxot[0]
10a
10b
10c
10d
10e
10f
10g
10h
7delay
gxot7d[7]
gxot7d[6]
gxot7d[5]
gxot7d[4]
gxot7d[3]
gxot7d[2]
gxot7d[1]
gxot7d[0]
10q
10r
10s
10t
10u
10v
10w
10x
gx[7]
gx[6]
gx[5]
gx[4]
gx[3]
gx[2]
gx[1]
gx[0]
10i
10j
10k
10l
10m
10n
10o
10p
gxot[7:0]
10 FIRST CALCULATION BLOCK

FIG. 6

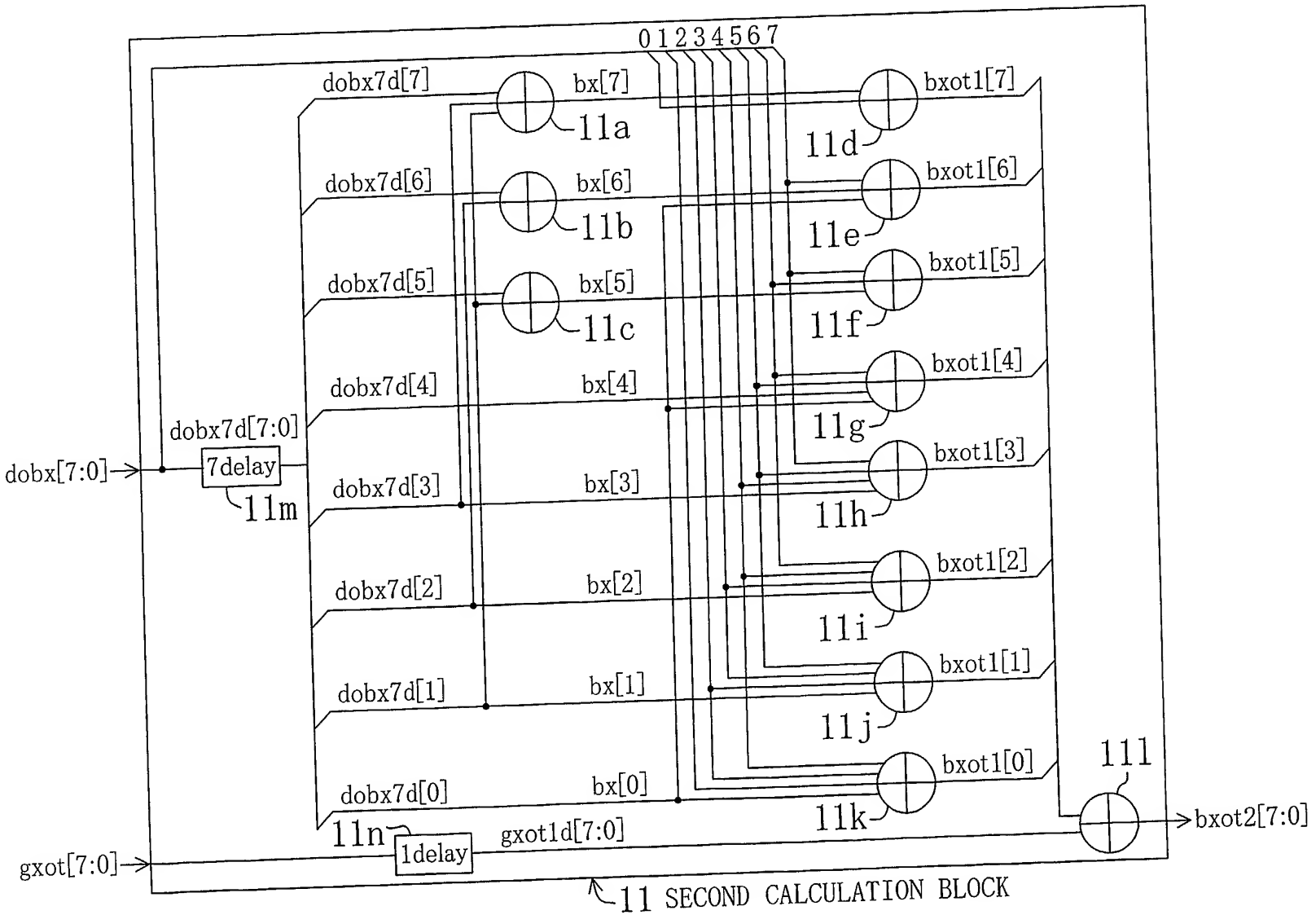
0 1 2 3 4 5 6 7
dobx7d[7]
bx[7]
11a
bxot1[7]
11d
dobx7d[6]
bx[6]
11b
bxot1[6]
11e
dobx7d[5]
bx[5]
11c
bxot1[5]
11f
dobx7d[4]
bx[4]
bxot1[4]
11g
dobx7d[7:0]
dobx[7:0]
7delay
11m
dobx7d[3]
bx[3]
bxot1[3]
11h
dobx7d[2]
bx[2]
bxot1[2]
11i
dobx7d[1]
bx[1]
bxot1[1]
11j
dobx7d[0]
bx[0]
bxot1[0]
11k
111
bxot2[7:0]
11n
1delay
gxot1d[7:0]
gxot[7:0]
11 SECOND CALCULATION BLOCK

FIG. 7A

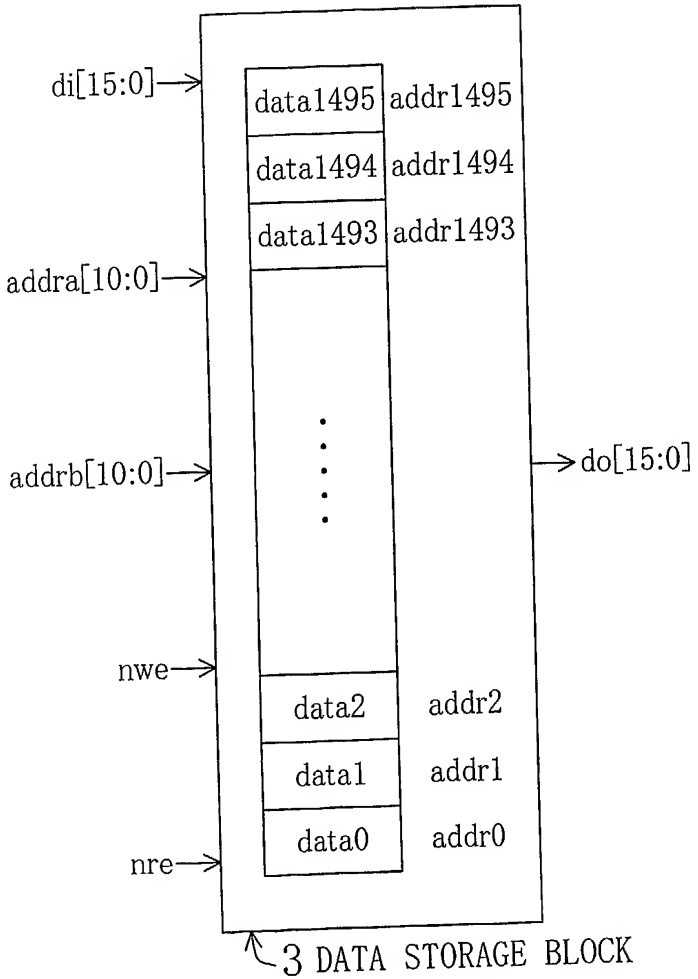

FIG. 7B

time	Read Address (addrb[10:0])	Write Address (addra[10:0])	di[15:0]	do[15:0]	nwe	nre
T1495	1494	1495	data1495	data1494	0	0
T1494	1493	1494	data1494	data1493		
⋮	⋮	⋮	⋮	⋮		
T2	1	2	data2	data1		
T1	0	1	data1	data0		
T0	1495	0	data0	data1495		

FIG. 8

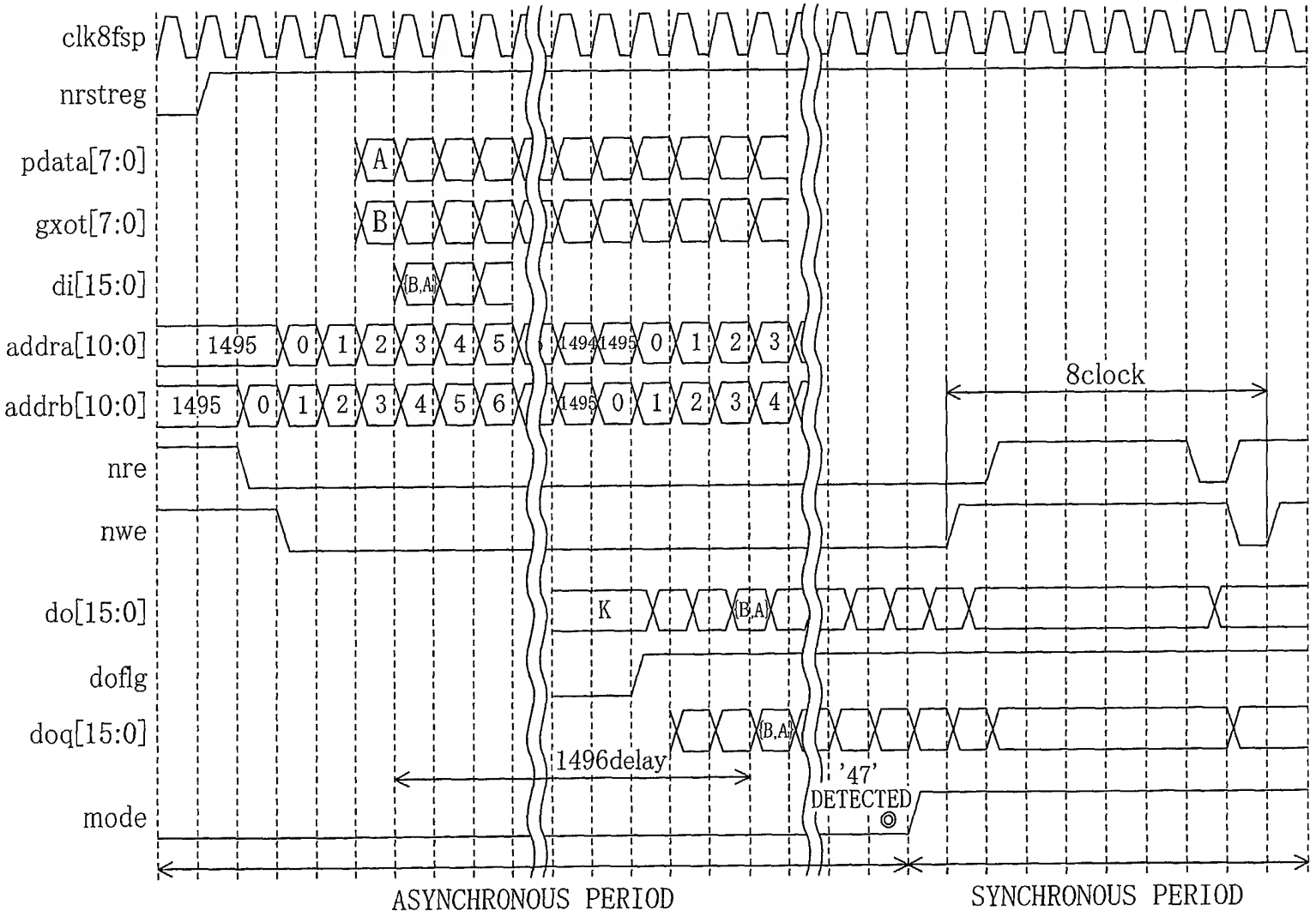
clk8fsp
nrstreg
pdata[7:0]
gxot[7:0]
di[15:0]
addra[10:0]
addrb[10:0]
nre
nwe
do[15:0]
doflg
doq[15:0]
mode
A
B
B,A
1495
0
1
2
3
4
5
6
1494
K
8clock
1496delay
'47'
DETECTED
ASYNCHRONOUS PERIOD
SYNCHRONOUS PERIOD

FIG. 9

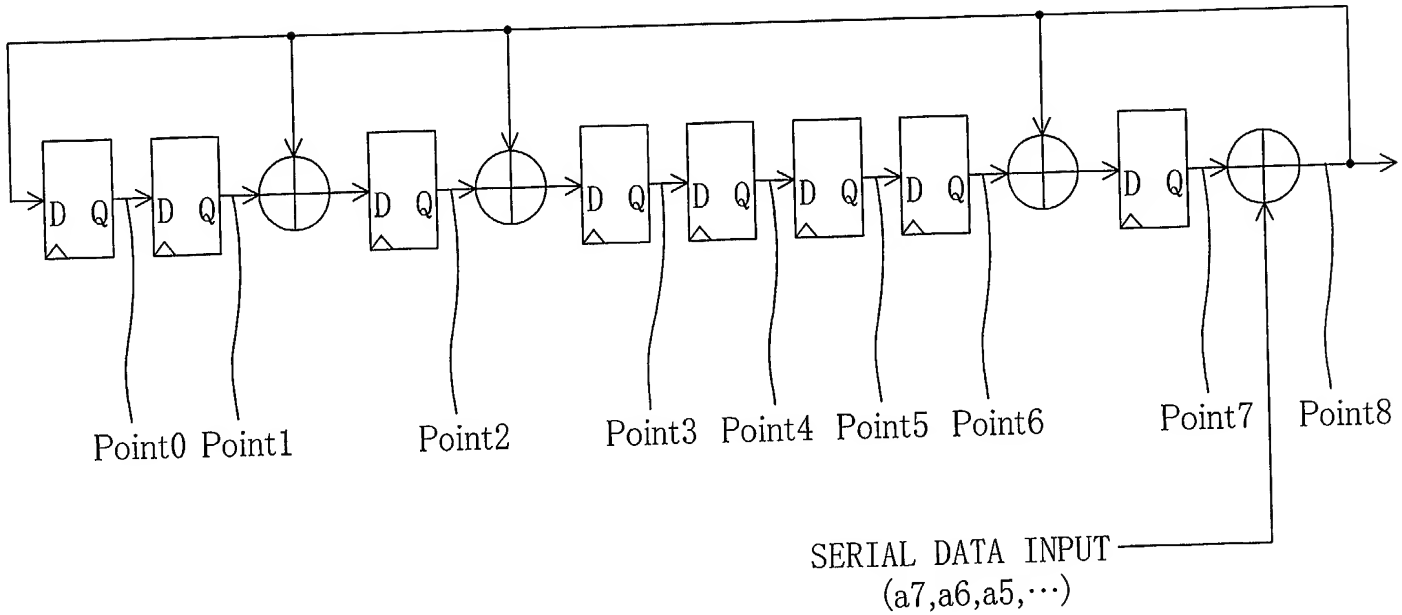
D Q
D Q
D Q
D Q
D Q
D Q
D Q
D Q
Point0
Point1
Point2
Point3
Point4
Point5
Point6
Point7
Point8
SERIAL DATA INPUT
(a7,a6,a5,···)

FIG. 10

time	Point8	Point7	Point6
1	X7+a7	X7	X6
2	X6+X7+a7+a6	X6+X7+a7	X5
3	X5+X6+X7+a7+a6+a5	X5+X6+X7+a7+a6	X4
4	X4+X5+X6+X7+a7+a6+a5+a4	X4+X5+X6+X7+a7+a6+a5	X3
5	X3+X4+X5+X6+X7+a7+a6+a5+a4+a3	X3+X4+X5+X6+X7+a7+a6+a5+a4	X2+X7+a7
6	X2+X3+X4+X5+X6+a6+a5+a4+a3+a2	X2+X3+X4+X5+X6+a6+a5+a4+a3	X1+X6+a6
7	X1+X2+X3+X4+X5+a5+a4+a3+a2+a1	X1+X2+X3+X4+X5+a5+a4+a3+a2	X0+X5+a5
8	X0+X1+X2+X3+X4+a4+a3+a2+a1+a0	X0+X1+X2+X3+X4+a4+a3+a2+a1	X4+X7+a7+a4

time	Point5	Point4	Point3
1	X5	X4	X3
2	X4	X3	X2+X7+a7
3	X3	X2+X7+a7	X1+X6+a6
4	X2+X7+a7	X1+X6+a6	X0+X5+a5
5	X1+X6+a6	X0+X5+a5	X4+X7+a7+a4
6	X0+X5+a5	X4+X7+a7+a4	X3+X6+X7+a7+a6+a3
7	X4+X7+a7+a4	X3+X6+X7+a7+a6+a3	X2+X5+X6+a6+a5+a2
8	X3+X6+X7+a7+a6+a3	X2+X5+X6+a6+a5+a2	X1+X4+X5+X7+a7+a5+a4+a1

time	Point2	Point1	Point0
1	X2	X1	X0
2	X1+X7+a7	X0	X7+a7
3	X0+X6+X7+a7+a6	X7+a7	X6+X7+a7+a6
4	X5+X6+a6+a5	X6+X7+a7+a6	X5+X6+X7+a7+a6+a5
5	X4+X5+a5+a4	X5+X6+X7+a7+a6+a5	X4+X5+X6+X7+a7+a6+a5+a4
6	X3+X4+a4+a3	X4+X5+X6+X7+a7+a6+a5+a4	X3+X4+X5+X6+X7+a7+a6+a5+a4+a3
7	X2+X3+X7+a7+a3+a2	X3+X4+X5+X6+X7+a7+a6+a5+a4+a3	X2+X3+X4+X5+X6+a6+a5+a4+a3+a2
8	X1+X2+X6+X7+a7+a6+a2+a1	X2+X3+X4+X5+X6+a6+a5+a4+a3+a2	X1+X2+X3+X4+X5+a5+a4+a3+a2+a1

FIG. 11

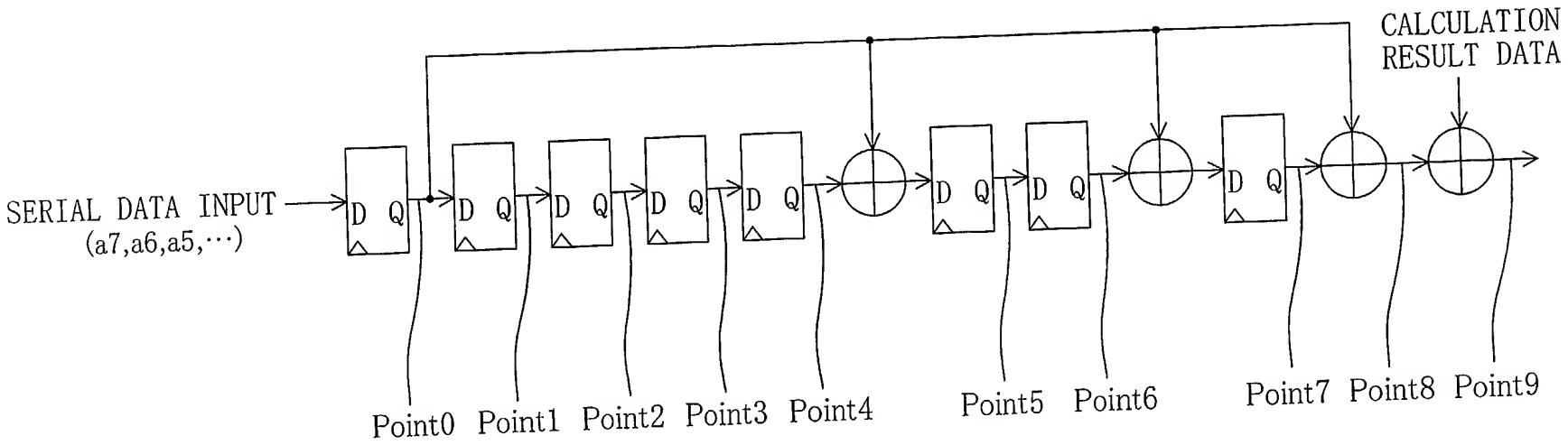
SERIAL DATA INPUT
(a7,a6,a5,···)
D Q
CALCULATION
RESULT DATA
Point0
Point1
Point2
Point3
Point4
Point5
Point6
Point7
Point8
Point9

FIG. 12

time	Point9	Point8	Point7	Point6	Point5
1	gxot1d7+X7+a7	X7+a7	X7	X6	X5
2	gxot1d6+X6+X0+a7	X6+X0+a7	X6+X0	X5	X4+X0
3	gxot1d5+X5+a7+a6	X5+a7+a6	X5+a7	X4+X0	X3+a7
4	gxot1d4+X4+X0+a6+a5	X4+X0+a6+a5	X4+X0+a6	X3+a7	X2+a6
5	gxot1d3+X3+a7+a5+a4	X3+a7+a5+a4	X3+a7+a5	X2+a6	X1+a5
6	gxot1d2+X2+a6+a4+a3	X2+a6+a4+a3	X2+a6+a4	X1+a5	X0+a4
7	gxot1d1+X1+a5+a3+a2	X1+a5+a3+a2	X1+a5+a3	X0+a4	a7+a3
8	gxot1d0+X0+a4+a2+a1	X0+a4+a2+a1	X0+a4+a2	a7+a3	a6+a2

time	Point4	Point3	Point2	Point1	Point0
1	X4	X3	X2	X1	X0
2	X3	X2	X1	X0	a7
3	X2	X1	X0	a7	a6
4	X1	X0	a7	a6	a5
5	X0	a7	a6	a5	a4
6	a7	a6	a5	a4	a3
7	a6	a5	a4	a3	a2
8	a5	a4	a3	a2	a1
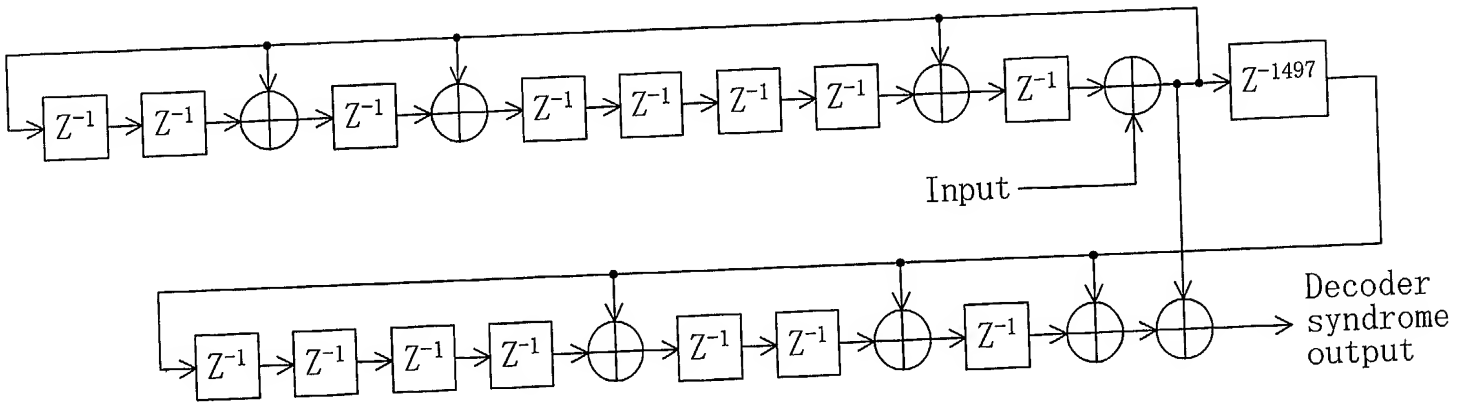
FIG. 13